



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/967,180	09/28/2001	2819	890	INTL-0551- US (P11110)	4	30	3

CONFIRMATION NO. 5958

FILING RECEIPT



OC000000007008497

Timothy N. Trop
TROP, PRUNER & NU, P.C.
STE 100
8554 KATY FWY
HOUSTON, TX 77024-1805

Date Mailed: 11/01/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Nathan Y. Moyal, Austin, TX;
James R. Feddeler, Austin, TX;
Michael Kent, Austin, TX;
Raha K. Prasun, Austin, TX;

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted 11/01/2001

Projected Publication Date: To Be Determined - pending completion of Missing Parts

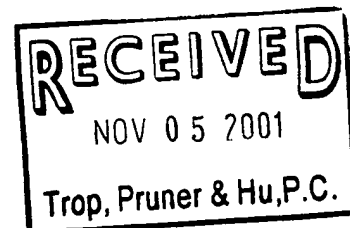
Non-Publication Request: No

Early Publication Request: No

Title

Resetting integrated circuits

Preliminary Class



RECEIVED
FEB - 6 2002
TO 2800 MAIL ROOM

DOCKET INFORMATION

Base Rate: _____

Due Date: _____

Action: _____

☒ Docket
☐ Pat. App

☒ Excel
☐ Abst./Title Pg

☐ Access
☐ Draw. [I/F]

**LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Office of Export Administration, Department of Commerce (15 CFR 370.10 (j)); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: RESETTING INTEGRATED CIRCUITS

INVENTORS: NATHAN Y. MOYAL, JAMES R. FEDDELER,
MICHAEL KENT, RAHA K. PRASUN

Express Mail No. EL911616535US

Date: SEPTEMBER 28, 2001

RESETTING INTEGRATED CIRCUITS

Background

This invention relates generally to integrated circuits and particularly to systems for starting up
5 integrated circuits.

During the start-up cycle of an integrated circuit, the supply voltage ramps up. A power-on reset circuit generally asserts reset whenever the supply voltage falls below a threshold. Moreover, the reset circuit asserts a
10 reset until the supply voltage has risen above the threshold for a suitable interval. The operation of the power-on reset circuit prevents various integrated circuits such as counters, phase-locked loops, filters, memories, flip-flops, and shift registers, as a few examples, from
15 operating improperly during start-up operation.

In some cases, such as those involving complex logic patterns or unexpected data patterns, an integrated circuit may be determined, incorrectly, to be in a ready state. It may be desirable to only release the circuit when it is in
20 its predetermined state. In some cases, the power-on reset circuits may release logic when the power supply has maintained its threshold level for a predetermined time even though the circuit's logic is not in its predetermined state. Conversely, the power-on reset circuit may

improperly release the integrated circuit because the logic is in the predetermined state even though the power supply level is still ramping.

Thus, there is a need for a system that does not
5 prematurely release an integrated circuit.

Brief Description of the Drawings

Figure 1 is a block diagram of one embodiment of the present invention;

10 Figure 2 is a block diagram of one embodiment of the present invention;

Figures 3a through 3c are timing diagrams for a plurality of signals in accordance with one hypothetical embodiment;

15 Figures 4a through 4c are timing diagrams for signals in accordance with another hypothetical embodiment;

Figure 5 is a block diagram for a chip for generating a power-on reset pulse in accordance with one embodiment of the present invention;

20 Figure 6 is a circuit diagram for one of the blocks shown in Figure 5 in accordance with one embodiment of the present invention; and

Figure 7 is a circuit diagram for additional blocks in the block diagram shown in Figure 5 in accordance with one
25 embodiment of the present invention.

Detailed Description

Referring to Figure 1, a functional block F may be controlled by a power-on reset circuit 10 to prevent its release for normal operation prior to the time that both
5 the power supply has stabilized and the logic in the functional block F has transitioned to predetermined logic states. The power-on reset circuit 10, in one embodiment, may include the decision logic 12, a latch 14, a pulse generator 16, and an amplifier 18a that couples a signal
10 feedback 20 back to the functional block F. The circuit 10 may be integrated on the same chip as the block F in one embodiment.

The functional block F may generate a plurality of output signals I_0 through I_N . Each of the signals is
15 received by the decision logic 12 so that the decision logic 12 can determine whether the logic of the functional block F is in the proper predetermined, initial states to begin normal operation.

During start-up, the signals I_0 through I_N may be in
20 some random state where it is highly probable that at least some of these signals are high and some are low. The decision logic 12 yields a low output to the S node of the latch 14 if one or more of the outputs I_0 to I_N of the functional block F is not in its predetermined state. The
25 decision logic tests the signals I_0 to I_N to determine whether those signals are in their proper initial states.

Meanwhile, the pulse generator 16 initially generates a high pulse into the R node of the latch 14 when the supply voltage is ramping up. The combination of a low S node and high R node may result in a reset signal being
5 sent to the functional block F through the amplifier 18a and the signal feedback 20. Thus, the pulse generator 16 may trigger the latch 14 to generate the reset signal to place the logic in the functional block into correct initial states.

10 The reset signal resets the logic in the functional block F to a desired predetermined state. As a result, the outputs I_0 through I_N yield known good states. When these good states are detected by the decision logic 12, this results in the latch 14 node S going high. The reset
15 signal remains active until the node S has become high, indicating that the functional block's logic is ready, and the pulse generator 16 signal has gone away, indicating that the power supply is now fully operational.

When the pulse generator 16 signal is gone and logic
20 indicates ready (S node = 1), normal chip operation begins in the functional block F. If the logic in the functional block F is not ready, for example due to long routing or for some other reason, the reset remains active, preventing normal operation of the function block F.

25 After the logic in the functional block F is released, the decision logic 12 may indicate a faulty ready state.

This may be the result of complex logic patterns or unexpected data patterns, as two examples. The reset signal is not improvidently activated since it is latched into a deactive state by the latch 14 until the power
5 cycles. The latch 14 releases from its deactivated state (no reset) only if the pulse generator 16 indicates that the power supply is ramping.

Referring, next to Figure 2, the functional block F in this example is a counter having logic in the form of a
10 plurality of flops only a few of which are shown. The reset signal (on feedback 20) to the flops is generated as soon as the pulse generator 16 is activated. The reset signal is active regardless of the indication from the logic within the functional block F. This is a desirable
15 property because during start-up it is possible to have faulty indicators from the functional block F.

The feedback signal 20 resets the counter to a predetermined state. The counter sends an "all high" signal to the AND gate 12a (which acts as the decision
20 logic) once all the flops are in their required logic states. Once the pulse generator 16 signal is gone ($R=0$), and the counter has indicated ready ($S=1$) the reset signal goes away. When the S and R inputs are zero or the R signal is one, the reset signal is active.

25 Potentially, the output of the AND gate 12a may be switched between low and high levels due to normal logic

operation of the counter which accidentally happens to instantaneously yield the correct initial, all high condition. However, the latch 14a will not reactivate because it has been latched to its deactive (no reset) state.

Referring to Figures 3a through 3c, the power supply signal Vcc shown in Figure 3a ramps up at 22 (when turned on) to a Vcc level 24. During the ramping (at 22), as shown in Figure 3b, the pulse generator 16 signal undergoes the transition to the high level 26 causing the functional block logic to go to "ready" (S=1), as indicated at 30 in Figure 3c. When the pulse generator 16 signal is high (Figure 3b) the logic AND is high (Figure 3c), the pulse generator 16 signal goes low (R=0) as indicated at 28. The pulse generator 16 signal being low causes the reset signal to go low releasing the logic in the functional block F, as indicated at 32 in Figure 3c. Logic glitches, indicated at 34 and 36, do not reactivate the reset signal, in one embodiment of the present invention, due to the latching action.

In the event that the I_0 through I_N AND signals indicate a high prior to the pulse generator 16 signal high 26, as indicated in Figures 4b and 4c, the circuit 10 still functions correctly in one embodiment. For example, as shown in Figure 4a, during the ramp indicated at 22, the pulse generator 16 signal goes high as indicated at 26 in

Figure 4b. Since the pulse generator 16 signal is high and the logic AND is high, the pulse generator 16 signal goes low as indicated at 28. The reset low results, causing the logic to release. Again logic glitches indicated at 34 and 5 36 do not reactivate the reset signal.

The use of the latch 14 may be advantageous in some embodiments since it useful for noise protection in low voltage applications. Noise on the supply or noise coupled from other lines may cause bouncing on critical nodes. 10 This bouncing may trigger the next stage to unexpectedly change state.

The functional blocks may be comprised of dynamic or static logic. In addition, the functional block may be a phase-locked loop (PLL). By allowing dynamic logic, the 15 state of the blocks that are used for normal operation may be monitored. Once they operate normally (reset is gone), they do not retrigger the reset pulse because of the latching operation.

Referring to Figure 5, in accordance with one 20 embodiment of the present invention, a particular pulse generator 16 is described. However, the present invention is in no way limited to the particular design depicted in Figure 5. A variety of pulse generator 16 designs may be utilized in the embodiments shown in Figures 1 and 2.

25 The pulse generator 16 shown in Figure 5 includes activation circuits 40 that handle the feedback of the

output pulse from pulse generator 16 along the line 55. In particular, the activation circuits 40 receive the feedback of the output pulse so that, once the pulse generator 16 signal goes away, the pulse generator 16 is not
5 inadvertently reactivated. The activation circuits 40 may also ensure that a predetermined supply voltage level is achieved before beginning the power on reset pulse generator 16 operation in one embodiment.

The activation circuits 40 provide outputs 53a and 53b
10 to the capacitor circuits 44. A variety of known capacitor circuits 44 may be utilized in some embodiments of the present invention. One capacitor circuit 44, shown in Figure 6, receives the supply voltage Vcc at the node 53a through the capacitor 56. The Vcc-connected capacitor 56
15 is pulled to Vcc. A capacitor 64, coupled to Vss (or ground), remains at ground initially.

The capacitor 56 slowly discharges to ground through the transistor 58 which acts as a current source. Meanwhile, the capacitor 64 begins to charge up to Vcc
20 through the low current transistor 60 and the pass gate transistor 62. Therefore, the capacitor circuits 44 count on the current to charge up or down each capacitor 56 or 64 above the trip point of the ensuing hysteresis sense stages 48. In addition, the capacitor 64, charging towards Vcc,
25 depends on the capacitor 56 that is charging to ground

before the capacitor 64 begins charging through the pass gate transistor 62.

After the supply voltage has reached its designated output level for the desired time period, the output 47a is high and the output 47b is low in one embodiment. These signals are conveyed to the hysteresis sense stages 48a and 48b. The output of the hysteresis sense stage 48a may be coupled to a logic functionality 52.

The logic functionality 52 determines whether the signal is at an appropriate level to accurately trigger the logic in the functional blocks being initialized. While a variety of different techniques may be utilized for testing the output of one or more hysteresis sense stages 48, in one embodiment, the most difficult logic to trigger may be emulated in the logic functionality 52. In some embodiments, the toughest logic is an inverter-like stage with stacked p-channel transistors because such a stage has particularly poor headroom.

If the power supply voltage level is too low, the decision logic 54 yields a pulse that may be applied as indicated in Figure 1 for example. The decision logic 54 receives signals from the hysteresis sense stages 48a and 48b. The decision logic 54 generates a high pulse if the ground connected capacitor 64 did not charge up to V_{cc} or the power connected capacitor 56 did not charge up to V_{ss} or the functional logic 52 did not pass the signal. The

pulse generator 16 continues during the power supply ramp up. When that ramp up is over for a sufficient period of time, the decision logic 54 causes the pulse generator 16 output to go away.

5 Figures 7 and 8 show activation circuits 40 in accordance with one embodiment. The activation circuit 40a receives the feedback signal 55a. In the case where the output pulse is low, meaning that the pulse generator 16 pulse has gone away because the desired power supply
10 conditions have been met, the inverter 64a inverts the low input signal 55a to a high output on the gate of the N-channel transistor 66a. This enables the transistor 66a to conduct. If the supply voltage (Vcc) is sufficient, the transistors 66a and 70a conduct.

15 Thus, the activation circuit 40a, in one embodiment, is not triggered until the supply voltage has reached a level sufficient to activate both transistors 66a and 70a. At this point the supply voltage should have reached a voltage level greater than two N-channel transistor
20 threshold voltages or in one embodiment approximately 1.4 volts.

 When the activation circuit 40a turns on, it shorts the capacitor node 53a in the ensuing capacitor circuit 44. In particular, the node 53a is pulled harder towards
25 ground. This pulls the output 47b harder towards ground and tends to latch the pulse generator 16 in its deactivated

state. In one embodiment, the transistor 70a may be stronger than the transistor 58.

Likewise, the circuit 40b, shown in Figure 8, receives the low input 55b and provides it to the gate of a P-channel transistor 66b. The P-channel transistor 66b turns on and turns on the transistor 70b when the threshold voltages of the transistors 66b and 70b are exceeded. When this happens, the transistor 70b decouples the capacitor 64 from the rest of the circuit and effectively latches a high output 47a through the node 53b.

Thus, the circuits shown in Figures 7 and 8 tend to latch the capacitor circuits 44 (shown in Figure 6) into their deactivated states (indicating that the output pulse is no longer needed). In particular, the circuits 40 make it harder to retrigger the pulse generator 16 prior to a power cycle.

Latching the critical nodes 53 from one threshold voltage above V_{ss} to V_{ss} may increase noise immunity in some embodiments. This may be useful, for example, for noise protection in low voltage applications, such as .7 volt applications. When the supply capacitor 56 is connected through a diode connected transistor 58 to ground, noise on the voltage supply (V_{cc}) can cause the diode node 53a to bounce. This bouncing can trigger a stage 48. The likelihood of this occurring may be reduced by using the latching operation in one embodiment.

Likewise, the capacitors 56 and 64 may be switched to the supply voltage and may be used as decoupling capacitors on the voltage supply in one embodiment. This decoupling may reduce supply noise. In addition, without the feedback
5 55, current may pass through the diode/capacitor 56 combination in the circuit 44. This current may increase the power consumption under supply noise. By shorting the diode connected transistor 58, this power consumption may be reduced.

10 The use of two threshold voltage activation circuits 40 may, in some embodiments, make it less likely that the latching starts prior to the time when the logic is operational (one threshold voltage). In addition, the charging capacitors 56 and 64 are typically used for the
15 power-on reset application only. In the embodiment shown in Figures 5 through 8, the capacitors 56 and 64 may also be used for supply decoupling. Therefore, the same component may be utilized for two different purposes, reducing layout overhead, in some embodiments.

20 While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall
25 within the true spirit and scope of this present invention.

What is claimed is:

1 1. A method comprising:
2 determining whether logic in a functional block
3 is in a predetermined, initial state; and
4 releasing the logic to begin operation after a
5 supply voltage reaches a predetermined level and the logic
6 is in its predetermined, initial state.

1 2. The method of claim 1 including generating a
2 pulse to indicate that the supply voltage is ramping up.

1 3. The method of claim 2 including resetting said
2 logic to its predetermined initial state in response to
3 said pulse.

1 4. The method of claim 3 including indicating when
2 said supply voltage has reached its predetermined level and
3 providing a signal to a latch in response thereto.

1 5. The method of claim 4 including determining
2 whether said logic is in its predetermined initial state
3 and if so, providing a signal to said latch.

1 6. The method of claim 5 including stopping the
2 generation of a signal to reset said logic to its initial
3 state after said logic has provided a signal to said latch
4 indicating that the logic is in its predetermined initial

5 state and the supply voltage has reached its predetermined
6 level.

1 7. The method of claim 6 including preventing said
2 latch from thereafter changing state until the power supply
3 cycles again.

1 8. The method of claim 1 including testing the
2 output of the functional block using decision logic which
3 checks to determine whether the signals indicate that the
4 logic is in its predetermined, initial state.

1 9. The method of claim 1 including generating a
2 reset signal, in response to the ramping up of the supply
3 voltage, that resets logic in the functional block to its
4 predetermined, initial state.

1 10. The method of claim 1 including providing a reset
2 signal to dynamic logic.

1 11. The method of claim 10 including preventing said
2 dynamic logic from reactivating said reset signal.

1 12. An integrated circuit comprising:
2 a functional block including logic to generate
3 a plurality of signals; and

4 decision logic coupled to receive said signals to
5 determine whether the functional block logic is in a
6 predetermined, initial state and to generate an output
7 signal indicative of whether the functional block logic is
8 in the predetermined, initial state.

1 13. The integrated circuit of claim 12 including a
2 latch coupled to the output signal to generate a reset
3 signal to reset the functional block logic to the
4 predetermined, initial state.

1 14. The integrated circuit of claim 13 including a
2 pulse generator to supply a pulse to said latch indicative
3 of whether the supply voltage is at a predetermined initial
4 level.

1 15. The integrated circuit of claim 14 wherein said
2 latch attempts to reset the functional block logic to the
3 predetermined, initial state until said pulse generator
4 signal indicates that the supply voltage is at the
5 predetermined initial level and said decision logic
6 indicates that the functional block logic is in its
7 predetermined, initial state.

1 16. The integrated circuit of claim 15 including a
2 pulse generator to indicate that the supply voltage is
3 ramping up.

1 17. The integrated circuit of claim 16 wherein said
2 latch latches said reset signal in a deactivated state
3 wherein the reset signal does not reset said functional
4 block logic until the power supply cycles again.

1 18. The integrated circuit of claim 17 including
2 dynamic logic in said functional block.

1 19. The integrated circuit of claim 18 wherein said
2 latch prevents said dynamic logic from reactivating said
3 reset signal.

1 20. The integrated circuit of claim 19 wherein said
2 pulse generator enables the latch to generate a reset
3 signal to said functional block logic and thereafter, said
4 decision logic determines whether said functional block
5 logic is in its predetermined, initial state.

1 21. An integrated circuit comprising:
2 a power on reset pulse generator to generate an
3 output pulse until the supply voltage reaches a
4 predetermined level; and

5 a latch coupled to said generator to output a
6 signal indicative of whether a supply voltage has reached a
7 desired level.

1 22. The integrated circuit of claim 21 including a
2 functional block including logic to generate a plurality of
3 signals and decision logic coupled to receive said signals
4 to determine whether the functional block logic is in a
5 predetermined, initial state and to generate an output
6 signal indicative of whether the functional block logic is
7 in the predetermined, initial state.

1 23. The integrated circuit of claim 22 wherein the
2 output signal from said decision logic is coupled to said
3 latch.

1 24. The integrated circuit of claim 21 including a
2 functional block including logic, said circuit further
3 including a latch to output a signal indicative of whether
4 a supply voltage has reached a desired level and whether
5 the logic in the functional block is in a predetermined,
6 initial state.

1 25. The integrated circuit of claim 21 including a

2 functional block including logic having a predetermined,
3 initial state, the latch output signal coupled to said
4 functional block logic.

1 26. The integrated circuit of claim 25 wherein said
2 latch attempts to reset the functional block logic to the
3 predetermined, initial state until the pulse generator
4 pulse indicates that the supply voltage is at a
5 predetermined initial level and the functional block logic
6 is in its predetermined, initial state.

1 27. The integrated circuit of claim 26 wherein said
2 latch latches the output of said latch in a deactivated
3 state wherein the output of the latch does not reset the
4 functional block logic until the power supply cycles again.

1 28. The integrated circuit of claim 27 wherein said
2 functional block includes dynamic logic.

1 29. The integrated circuit of claim 28 wherein said
2 latch prevents the dynamic logic from altering the output
3 signal from said latch.

1 30. The integrated circuit of claim 29 wherein said
2 pulse generator enables the latch to generate a reset
3 signal to the functional block logic and thereafter

- 4 determine whether the functional block logic is in the
- 5 predetermined, initial state.

RESETTING INTEGRATED CIRCUITS

Abstract of the Disclosure

An integrated circuit may be initialized by
5 determining that the supply voltage is ramping up and
resetting logic in the integrated circuit to a
predetermined initial state using a reset signal. After
the logic is determined to be in its initial state and the
supply voltage is established, the reset signal may be
10 latched off.

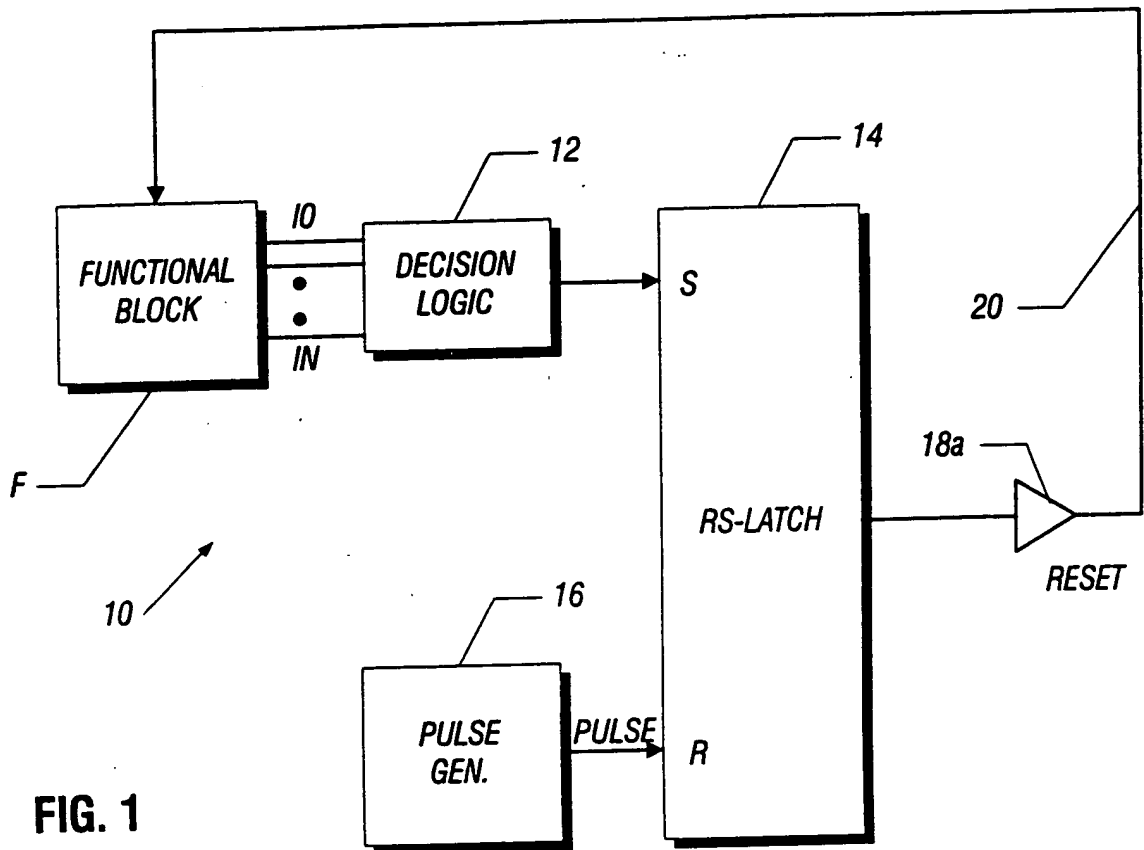


FIG. 1

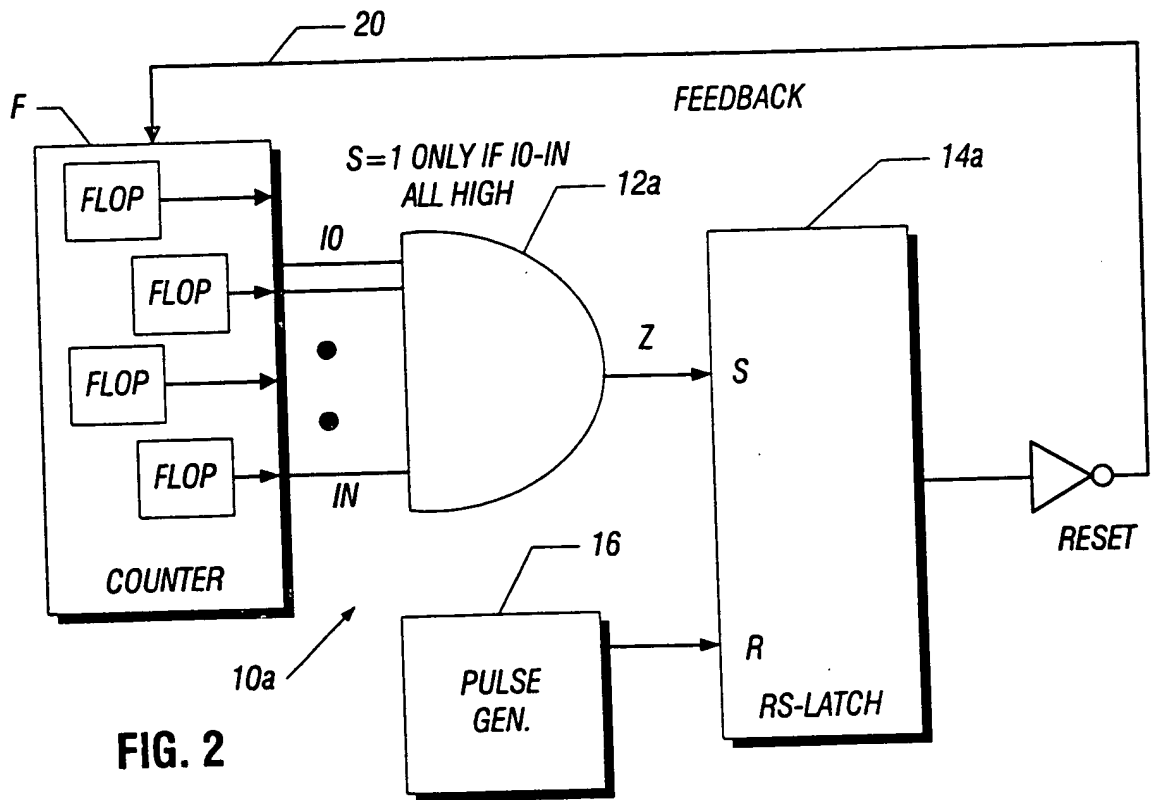
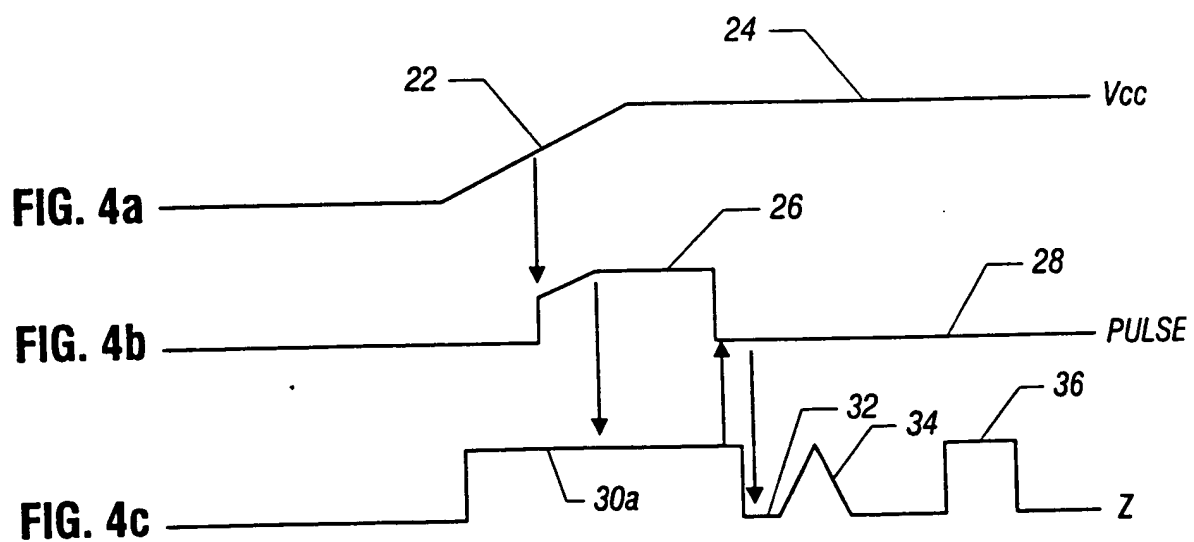
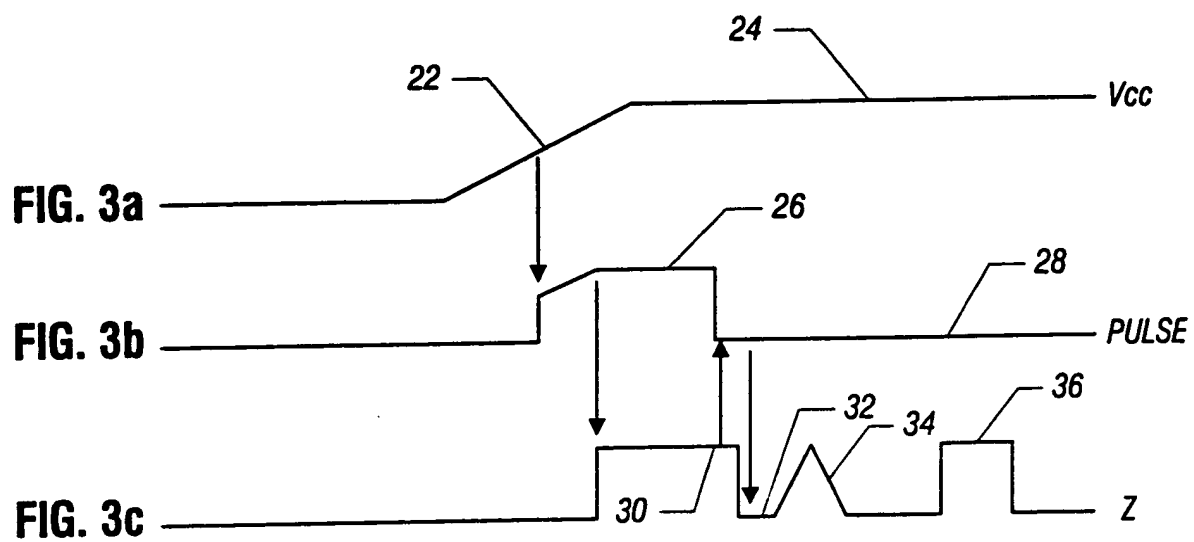


FIG. 2



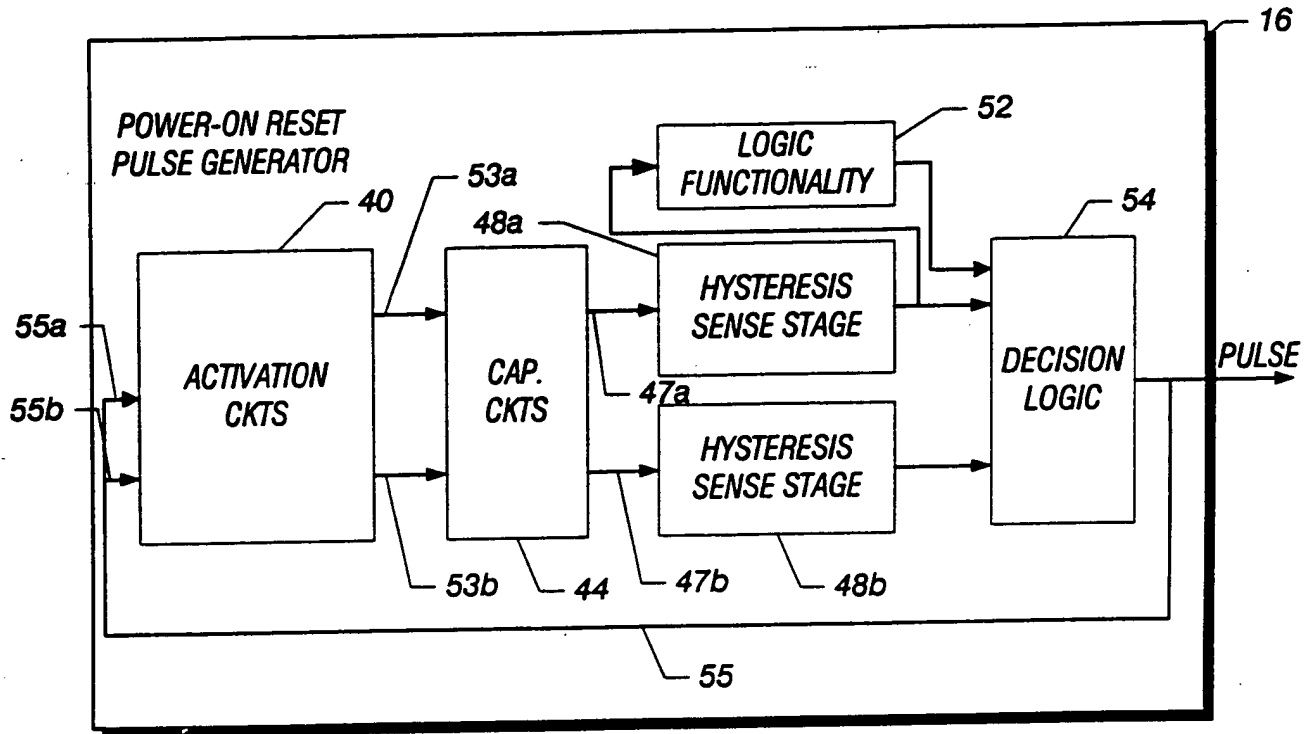


FIG. 5

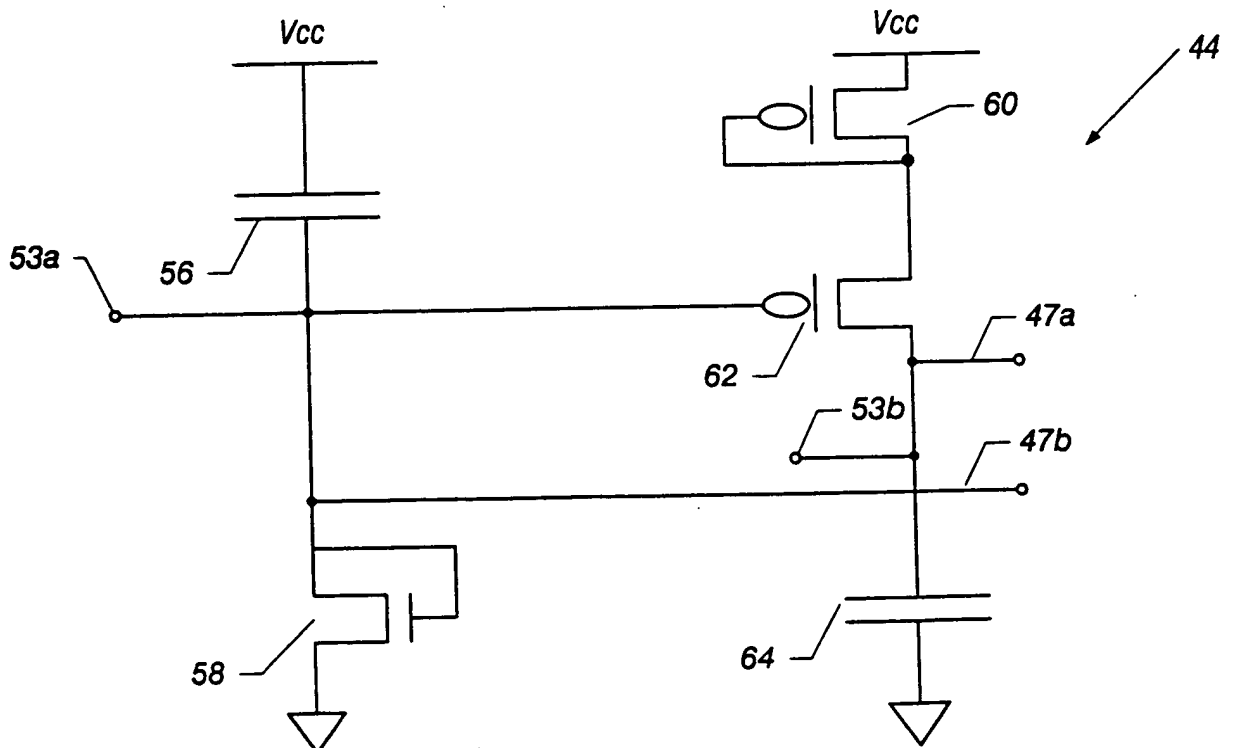


FIG. 6

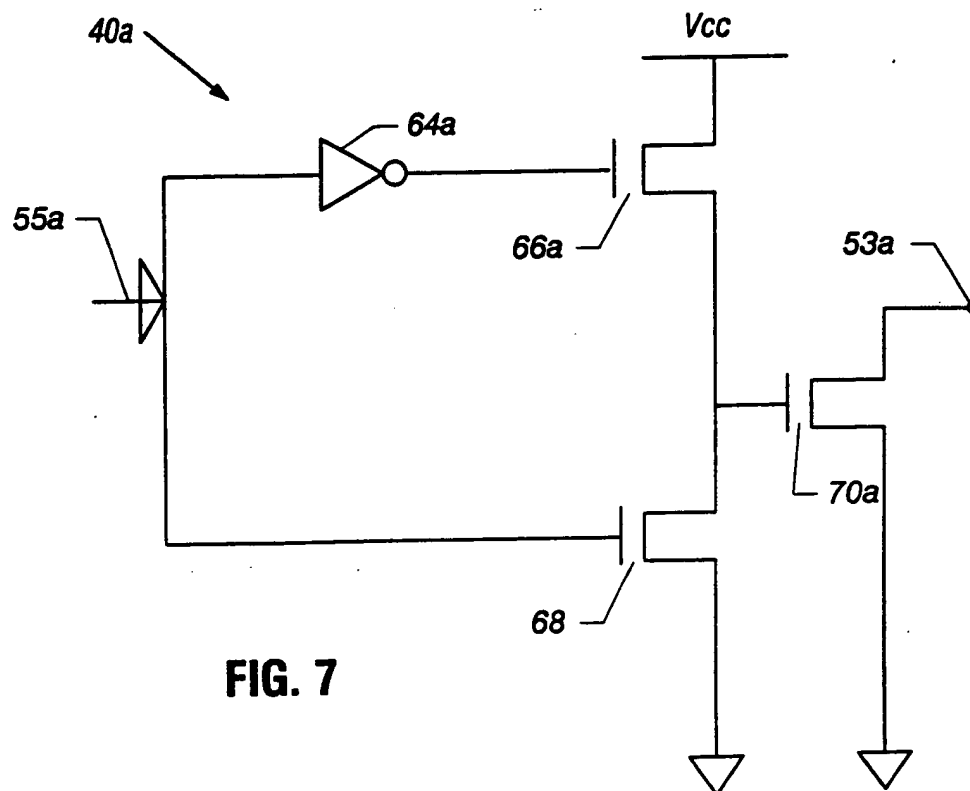


FIG. 7

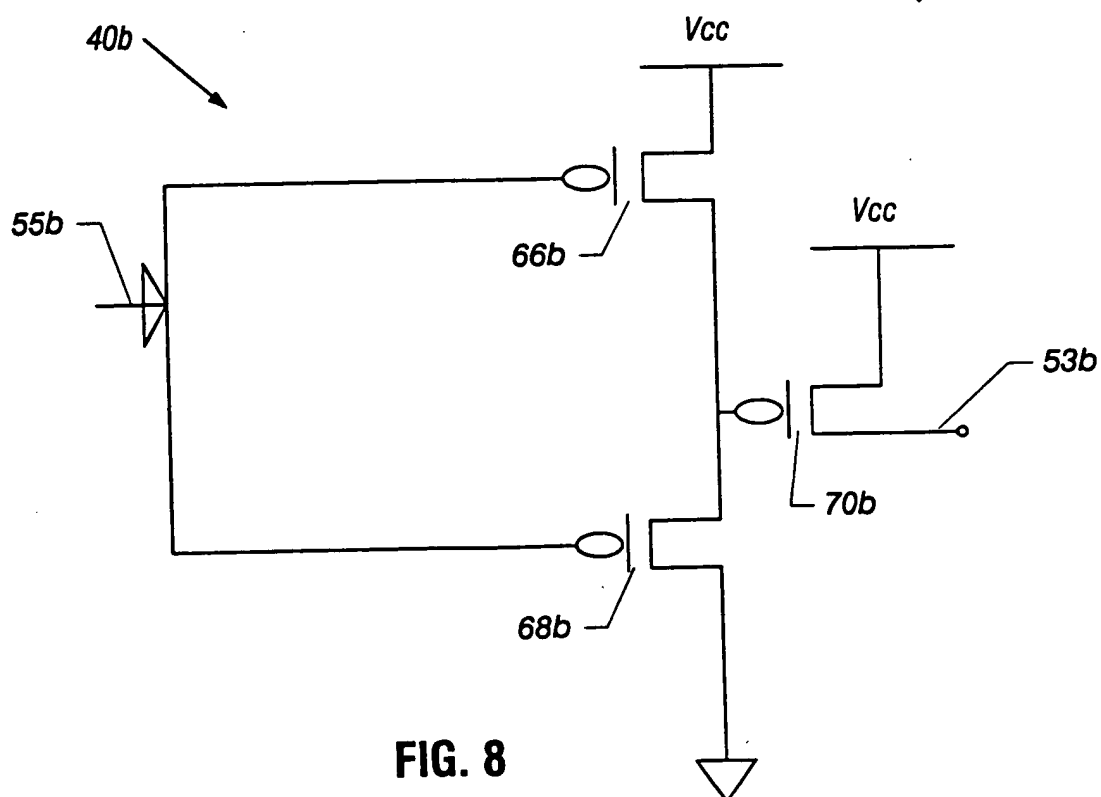


FIG. 8